

Jaipur Institute of Technology Group of Institutions

/ Jaipur - Near Mahindra SEZ Kalwara, Ajmer Road



LAB-MANUAL

VI SEM EE

Analog electronics lab

Sl.	Topic.	Page No
1.	Syllabus	5
2.	Overview of analog electronics lab.	7
3.	Cycle of experiments.	9
4.	Diode clipping and clamping circuits.	10
5.	Centre tap full wave rectifier and bridge rectifier.	15
6.	BJT common emitter amplifier using voltage divider bias with and without feedback.	19
7.	Complementary symmetry class B push pull power amplifier.	23
8.	BJT Darlington emitter follower with and without bootstrapping.	25
9.	Series Voltage Regulator using Zener diode and power transistor.	28
10.	Hartley Oscillator and Colpitts Oscillator.	30
11.	Crystal oscillator.	34
12.	Characteristics of a JFET.	36
13.	Characteristics of N-channel MOSFET.	38
14.	Common source JFET/MOSFET amplifier	40
15.	RC-Phase shift oscillator using FET.	44
16.	Viva questions	46

ANALOG ELECTRONICS LABORATORY

As per Choice Based Credit System (CBCS) scheme] SEMESTER – III (EC/TC)

Laboratory Code 15ECL37 IA

Marks 20

Number of

Lecture

Hours/Week 01Hr Tutorial

(Instructions)

+ 02 Hours

Laboratory Exam Marks 80

CREDITS 02 Exam Hours 03

Course objectives:

This laboratory course enables students to get practical experience in design, assembly, testing and evaluation of

- Rectifiers and Voltage Regulators.
- BJT characteristics and Amplifiers.
- JFET Characteristics and Amplifiers.
- MOSFET Characteristics and Amplifiers
- Power Amplifiers RC-Phase shift, Hartley, Colpitts and Crystal Oscillators

NOTE: The experiments are to be carried using discrete Components only. Revised

Bloom's

Taxonomy

(RBT) Level

1. Design and set up the following rectifiers with and without filters and to determine ripple factor and rectifier efficiency:

(a) Full Wave Rectifier (b). Bridge Rectifier L1 - Remembering

L2 - Understanding

L3 - Applying

L4 - Analyzing

2. Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative). L1 - Remembering

L2 - Understanding

L3 - Applying

L4 – Analyzing

3. Conduct an experiment on Series Voltage Regulator using Zener diode and power transistor to determine line and load regulation characteristics. L2 - Understanding

L3 – Applying

L4 - Analyzing

4. Realize BJT Darlington Emitter follower with and without bootstrapping and determine the gain, input and output impedances. L2 - Understanding

L3 – Applying

L4 - Analyzing

5. Design and set up the BJT common emitter amplifier using L2 - Understanding

L3 - Applying

voltage divider bias with and without feedback and determine the gain- bandwidth product from its frequency response. L4 – Analyzing

L5 - Evaluating

6. Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor. L1 - Remembering

L2 - Understanding

L3 - Applying

L4 - Analyzing

7. Design, setup and plot the frequency response of Common

Source JFET/MOSFET amplifier and obtain the bandwidth. L2 - Understanding

L3 - Applying

L4 – Analyzing

L5 – Evaluating

8. Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor. L1 - Remembering

L2 - Understanding

L3 - Applying

L4 - Analyzing

9. Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency. L2 - Understanding

L3 - Applying

L4 – Analyzing

L5 – Evaluating

10. Design and set-up the RC-Phase shift Oscillator using FET, and calculate the frequency of output waveform. L2 - Understanding

L3 - Applying

L4 – Analyzing

L5 – Evaluating

11. Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation.

(a) Hartley Oscillator (b) Colpitts Oscillator L2 - Understanding

L3 - Applying

L4 – Analyzing

L5 – Evaluating

12. Design and set-up the crystal oscillator and determine the frequency of oscillation. L2 - Understanding

L3 - Applying

L4 – Analyzing

L5 – Evaluating

ANALOG ELECTRONICS LABORATORY:

Analog Electronics as the name suggests deals mainly with Analog signals. Analog electronic circuit design is one of the important and challenging fields in Electronics. The area of analog electronics is one of the vast and complex areas in VLSI circuits design. A signal which is having different values at different instants of time is referred to as an analog signal. Analog electronic circuits can be designed and tested for their performance using the tools like PSPICE, Cadence, etc.. Many analog circuits are available in the form of IC chips.

During this Lab course simple analog electronic circuits are designed using discrete components like Resistors, Capacitors, Inductors, PN junction diodes and Transistors (BJT's, FET's, etc.), etc.. These designed circuits are tested and verified for their performance under the laboratory conditions using power sources like DC Power supply, AC sources like function generators. Their input and output parameters like input waveforms, output waveforms, input and output current and voltage readings, the impedance or resistance offered by the circuit, etc are analyzed by using measuring instruments like multimeter and CRO's. The captured values from the instruments are noted and used for further calculations.

Analog electronics laboratory course flow:

To start with this laboratory session, initially all students are trained to use the measuring instruments like Multi-meter and CRO. Thorough understanding of CRO is mandatory for proceeding with the courseware. The function or signal generators which generate the analog signals of desired frequency and amplitude (frequency and voltage levels) and usage of power supply etc are made familiar to the students. Reading the values of the passive components like resistor, capacitor, etc. using color code is taught.

After completing the above exercise, the design aspects of analog circuits are carried out. Thereafter the conduction of the experiments are started to verify and test the performance of the designed analog circuits. The input and generated output waveforms are sketched and the results are noted for further calculations.

Instructions to the students are given in the start of this document which they are advised to read before they start conducting experiments.

Instructions before Starting the Experiment

1. Students are expected to study the circuit, theory and procedures, expected output before doing the experiment.
2. Adjustment of signal generator: - Before connecting the signal generator to the circuit check the followings.
 - a. Set the shape of the waveform (sinusoidal),
 - b. Set the frequency using coarse and fine adjustments.
 - c. Set the offset adjustments. Set the CRO in DC mode and ensure the waveform is symmetry in both positive and negative cycle. If not , adjust it using the DC offsetting potentiometer
 - d. Set the voltage magnitude using Vcourse settings and Vfine adjustments.
3. Adjustment of CRO:
 - a. Select the right voltage and time scale to get the proper waveform
 - b. For clipper and clamper circuits, observe the waveform in DC mode only
 - c. Set the input waveform mainly for offset setting in DC mode only.
 - d. Before measurement, ensure X & Y are in calibrated mode (if provided externally)
 - e. Ensure that Channel selection and trigger mode are properly set.
 - f. In case of two channels do not mix the signal and ground terminals.
4. Multi-meter adjustments:-
 - a. Set the right mode before taking the readings.
 - b. For current reading, connect the multimeter in mA (or A) mode to the circuit before switching on the supply. Do not remove the current meter when the supply is on. Check for ac and dc modes as required.
 - c. For voltage reading ensure that proper ac or dc setting.
 - d. Use the proper leads for the measurement. Wrong cables damage the instrument.
5. After adjusting the input voltage, check the circuit connections before turning the power on.
6. Ensure that the circuit has one ground.
7. Don't pull out the connections with the power supply on.

CYCLE – I

1. Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative).

2. Design and set up the following rectifiers with and without filters and to determine ripple factor and rectifier efficiency:

(a). Full Wave Rectifier (b). Bridge Rectifier

3. Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain- bandwidth product from its frequency response.

4. Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency

CYCLE – II

5. Realize BJT Darlington Emitter follower with and without bootstrapping and determine the gain, input and output impedances.

6. Conduct an experiment on Series Voltage Regulator using Zener diode and power transistor to determine line and load regulation characteristics.

7. Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation. (a) Hartley Oscillator (b) Colpitts Oscillator

8 Design and set-up the crystal oscillator and determine the frequency of oscillation.

CYCLE – III

9 Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.

10 Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.

11 Design, setup and plot the frequency response of Common Source JFET/MOSFET amplifier and obtain the bandwidth.

12 Design and set-up the RC-Phase shift Oscillator using FET, and calculate the frequency of output waveform.

EXPERIMENT 1

CLIPPER & CLAMPER CIRCUITS

1.1 CLIPPER

Aim: - Conduct experiment to test diode clipping (single/double ended).

Components required: - Switching diode – 1N4007, Resistors 10K/1k Signal generator, Variable DC supply Capacitor 1uf/10uf 20V, bread board, Wires, CRO & multimeter for testing

Theory:- Clippers are networks that employ diodes to clip away portions of an input signal without distorting the remaining part of the applied waveform. These clipper circuits transfer a selected portion of the input waveform to the output Diode clipping circuits are used to prevent a wave form from exceeding some particular limit either negative or positive or both. This is achieved by connecting the diode in serial or in parallel circuit. Variable DC voltage is connected in the circuit to achieve required level of clipping. By using different level DC voltages, it is possible to get different level of clipping in positive and negative side. These clipper circuits are also called as limiters.

Following are few types of clipper circuits

1. Single ended (positive or negative) and double ended clipping
2. Series or parallel based on the construction.

Peak detection is possible by connecting a suitable capacitor across the output of single ended clipping circuit. The capacitor charging time to be fast and discharging time to be slow so that capacitor holds the maximum value.

DESIGN:

Assume Forward Resistance of Diode, $R_f = 100 \Omega$; Reverse Resistance of Diode, $R_r = 1M\Omega$

The series resistance is calculated such that $R \gg R_f, R_r \gg 100 \gg 106 \gg 10K$

Note: If you are using 1N4001 R_f and R_r may be assumed to be 30Ω and $300K \Omega$ respectively and $R = 3.3 K \Omega$

The series resistor is used to limit the current through the diode.

Circuit Diagram

Figure 1: Positive shunt clipper

If the output to be clipped above 2 V, $V_o (\max) = +2 V$

From the Fig.1 observe that when the diode is ON $V_o (\max) = V_D + V_{ref}$ where V_D is Diode

Cut-in Voltage which is equal to 0.6 V for 1N4007 (Silicon diode)

$$\text{Hence } V_{ref} = V_o (\max) - V_D = 2 - 0.6 = 1.4 V$$

Make sure that the amplitude of the input sinusoidal signal is more than ± 2 Volts.

Figure 2: Negative shunt clipper

If the output to be clipped below ± 2 Volts.

From the Fig.2 observe that when the diode is ON $V_o(\min) = -V_D - V_{ref} = -2 \text{ V} = -0.6 - V_{ref}$;

$$-V_{ref} = 2 - 0.6 = 1.4 \text{ V} \quad V_{ref} = 1.4 \text{ V}$$

Make sure that the amplitude of the input sinusoidal signal is more than ± 2 Volts.

Figure 3 : Positive series clipper

Figure 4: Negative series clipper

Figure 5: Double ended clipper with independent voltage levels

If the clipping the signal is required below 2 Volt and above 4 Volt then the design is as follows.

- $V_o \max = 4 \text{ V}$,
 $V_o \max = V_{R1} + V_D$; $V_{R1} = V_o \max - V_D = 4 - 0.6$; $V_{R1} = 3.4 \text{ V}$
- $V_o \min = 2 \text{ V}$
 $V_o \min = V_{R2} - V_D$; $V_{R2} = V_o \min + V_D = 2 + 0.6$; $V_{R2} = 2.6 \text{ V}$

Figure 6: Double ended clipper with symmetrical voltage levels

If we need to generate a symmetrical clipping circuit with clipping voltage $V_0 = \pm 4$ Volts,

$$V_o \max = V_{R1} + V_D = 4 \text{ V}; \quad V_{R1} = 4 - 0.6 = 3.4 \text{ V}$$

$$V_o \min = -V_D - V_{R2} = -4 \text{ V}, \quad V_{R2} = 4 - 0.6 = 3.4 \text{ V}$$

1.2 CLAMPER

Aim: - Conduct experiment to test diode clamping circuits (positive/negative).

Components and equipments required: - Switching diode: 1N4007, Resistors 100 K Ω , Capacitor 1 μ f, 20V; Signal generator, Variable dc supply , Bread board, CRO.

Theory:- Clamper is a circuit that "clamps" a signal to a different dc level without changing the appearance of the applied signal. The different types of clampers are positive negative and biased clampers. A clamping network must have a capacitor, a diode and a resistive element. The magnitude R and C must be chosen such that the time constant RC is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non-conducting. By connecting suitable DC voltage in series with the diode, the level of swing can be varied.

Circuit Diagram

Positive peak clamper

Figure 1: Positive clamper.

Figure 2: Positive clamper negative peak clamped.

Design: $V_{o,max} = V_{dc} + V_D$; $V_D = 0.6V$ (Silicon diode), $V_{dc} = V_{o,max} - V_D$

To clamp the positive peak of a sine wave of 10 V (P – P) at +3V, we need $V_{dc} = 3 - 0.6 = 2.4 V$

Note: Changing this voltage changes the clamping level.

Let $f = 1KHz$. $T = 1msec$. Let $R = 10K\Omega$ (design procedure is same as that of clipper)

For the circuit to perform satisfactorily $RC = 10T$

Therefore $C = 10T / R = 10 \times 1ms / 10K\Omega$; $C = 1.0 \mu F$

Figure 3: Positive clamper to clamp negative peak

$V_{o,max} = V_{dc} - V_D$; Assume we need to clamp the negative peak to -3V, ie., $V_{o,max} = -3V$

$V_{dc} = V_{o,max} + V_D$,

$V_{dc} = -3 + 0.6 = -2.4V$ (Note: Changing this voltage changes the clamping level.) The design of R and C is as mentioned in earlier circuit

Procedure:-

1. Set up the circuit on the bread board.
2. Switch on the signal generator and set voltage 10V P-P and frequency 1 KHz.
3. Using CRO measure the output wave form and see that it matches with required wave form.
4. Repeat this for other clipper and clamper circuits.

Result: - All types of clipper and clamper circuits are tested and output wave form matches with the expected waveform.

EXPERIMENT 2

RECTIFIERS

Aim: Design and set up the following rectifiers with and without filters and to determine ripple factor and rectifier efficiency: (a). Full Wave Rectifier (b). Bridge Rectifier

2.1 FULL WAVE RECTIFIER

Components and equipments required: Center tapped transformer 12 – 0 – 12. IN4007 diodes – 2 nos, Resistors – 10 Ω - 2nos, DRB, Multimeter, CRO and Bread board.

Theory:

Full wave bridge rectifier

Centre tap full wave rectifier

Working principle of centre tap full wave rectifier

During positive half cycle of the input voltage, the diode D1 is forward biased and conducts and diode D2 is reverse biased and will not conduct. The current will flow through the direction A-B-C-D-E. During negative half cycle diode D2 is forward biased and conducts. Diode D1 is reverse biased and will not conduct. The current will flow through the direction F-B-C-D-E. Therefore during both half cycles i.e., positive and negative half cycles the output current will be in only one direction

Working principle of full wave bridge rectifier

During positive half cycle of the input voltage, the diode D1 and D3 is forward biased and both diodes will conduct and diode D2 and D4 is reverse biased and will not conduct. The current will flow through the direction A-B-C-D-E-F-G.

During negative half cycle, the diode D2 and D4 is forward biased and both diodes will conduct and diode D1 and D3 is reverse biased and will not conduct. The current will flow through the direction G-F-C-D-E-B-A. Therefore during both half cycles i.e., positive and negative half cycles the output current will be in only one direction i.e., from point C to D.

Design: (Common for both rectifiers)

For the transformer, primary voltage $V_P=230\text{ V}$

Secondary voltage $V_S=12\text{ V}$

Voltage across diode $V_D = 0.6\text{ V}$ (Silicon transistor)

For a diode current of 10 mA , i.e., $I_D = 10\text{ mA}$

$R_L = [V_S - V_D] / I_D = [12 - 0.6] / 10\text{ mA} = 1.14\text{ K}\Omega$; choose $R_L = 1\text{ K}\Omega$

With capacitor filter, ripple factor

Allowing 3% ripple, i.e., $r=0.03$, $f = 50\text{ Hz}$, $R_L = 1\text{ K}\Omega$ we get $C = 96.225\mu\text{F}$, let $C=100\mu\text{F}$

$V_m = 12\sqrt{2} = 16.97\text{ V}$ (Maximum value of the sinusoidal voltage applied to the rectifier)

$V_{dc} = 2V_m/\pi = 10.8\text{ V}$ (For the rectifier without filter, Theoretical)

$I_{dc} = V_{dc}/R_L$ (DC Current through the load)

$I_{dc} = 10.8\text{ V}/47\Omega = 229.78\text{ mA}$ (Full Load current, min value of R_L shown in the Table, with $R_S=R_f=0$),

$P_{dc} = V_{dc}I_{dc}$ (Load Power)

$P_{ac} = V_S I_S$ (Power supplied by the transformer)

Ripple factor $\gamma = V_{ac}/V_{dc}$ (=1.21 Theoretical)

%Efficiency = P_{dc}/P_{ac} ((40.6%, Theoretical)

%Regulation = $E = (V_{NL}-V_{FL})/V_{FL}$

Circuit Diagram:

1. Center tap full wave rectifier with filter (remove C for rectifier without filter)
2. Full wave bridge rectifier with filter (remove C for rectifier without filter)

Expected waveform

Procedure:

1. Place the components on bread board and connect them as per circuit diagram.
2. Connect minimum output resistance and DRB in series
3. Switch on the input ac and note down readings. Tabulate the readings for different values of output resistor and find out ripple factor, load regulation, and efficiency.
4. Using CRO measure the output wave form and check whether it matches with required wave form.
5. Repeat this experiment for by connecting the suitable capacitor across the load to reduce the ripple to less than 3%

Observation

For both rectifiers use similar tabular column separately

Tabular column for rectifier without filter

RL Vm Use

CRO Vdc theoretical

$$V_{dc} = \frac{2V_m}{\pi} \quad V_{dc}$$

Practical Use multimeter in dc mode Vac practical Use multimeter in ac mode $\gamma =$

$$\frac{V_{ac}}{V_{dc}} \quad \eta =$$

$$\frac{V_{2dc}}{V_{2rms}}$$

1K?

2K?

3K?

4K?

5K?

Tabular column for rectifier with filter

RL Vm

Use CRO Vr,pp

Use CRO Vr,rms

Theoretical

Vr,rms =

$Vr,pp / 2 \sqrt{3}$ Vdc theoretical

Vdc =

$Vm - (Vr,pp/2)$ Vdc Practical

Use multimeter in dc mode $\gamma = Vr,rms/Vdc$ $\eta =$

$V2dc / V2rms$

1K?

2K?

3K?

4K?

5K?

Result:

EXPERIMENT 3

COMMON EMITTER AMPLIFIER

Aim: Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain- bandwidth product from its frequency response.

Components and equipments required: Transistor – SL100, Resistors - 470 Ω , 1K Ω , 10K Ω - 2nos, and 33K Ω , Capacitors 100 μf , 0.22 μf and 0.47 μf , Power Supply, 10Hz – 3MHz Signal generator, CRO, Connecting wires and Bread board/Spring board with spring terminals.

Design:

Transistor: SL100

Let $V_{CC} = 12\text{V}$; $I_C = 4.5 \text{ mA}$; $V_E = 1.2\text{V}$; $V_{CE} = 6\text{V}$; $h_{FE} = 100$.

Given $V_E = 1.2\text{V}$. Therefore $R_E = V_E / I_E \approx V_E / I_C = 266.67\Omega$; $R_E = 270\Omega$

Writing KVL for the Collector loop we get, $V_{CC} = I_C R_C + V_{CE} + V_E$

$\therefore R_C = (V_{CC} - V_{CE} - V_E) / I_C = (12 - 6 - 1.2)\text{V} / 4\text{mA} = 1.06\text{K}\Omega$; $R_C = 1 \text{ K}\Omega$

$h_{FE} R_E = 10R_2$

Assume $R_2 = 2.7\text{K}\Omega$,

$V_B = (V_{CC} \times R_2) / (R_1 + R_2)$

Hence $R_1 = 14.14 \text{ K}\Omega$; $R_1 = 15 \text{ K}\Omega$

Use $C_{C1} = 0.47\mu\text{F}$

Use $C_{C2} = 0.47\mu\text{F}$

Use $C_E = 47\mu\text{F}$

Circuit Diagram of amplifier without feedback.

Circuit Diagram of amplifier with feedback. (introduce a resistor in the emitter circuit)

Procedure:

Follow the same procedure for both circuits

1. After making the connections, switch on the D.C. power supply and check the D.C. conditions without any input signal and record in table below:

Parameter	VRC	VCE	VE	ICQ	VBE
Assumed	4.8V	6 V	1.2V	4.5 mA	0.6 V

Practical

2. Select sine wave input and set the input signal frequency $\geq 10f_1$ (Say = 10 KHz. This will be a convenient 'Mid – frequency').
3. Observe the input wave form and output wave form on a dual channel CRO.
4. Adjust the input amplitude such that the output waveform is just undistorted (or in the verge of becoming distorted). Measure the amplitude of the Input Signal now. This amplitude is the Maximum Signal Handling Capacity of your amplifier.
5. Decrease the input voltage to a convenient value such that the output is undistorted. Say 20mV. Measure the corresponding o/p voltage. Calculate mid-band gain, $AM = V_o (p-p) / V_{in} (p-p)$.
6. Keeping the input voltage constant, go on reducing the frequency until the output voltage reduces to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Lower Cut-off frequency (f_1).
7. Keeping the input voltage constant, go on increasing the frequency until the output voltage decreases to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Upper Cut-off frequency (f_2).
8. Thus you have pre-determined f_1 and f_2 . Find the amplifier band width, $BW = f_2 - f_1$
9. Determine Gain Bandwidth product (GBW product) which is a Figure of Merit of your amplifier as $GBW = AM \times BW$.
10. Now repeat the experiment by recording values of output voltage versus frequency keeping the input voltage at a constant value convenient to you. You should take at least 5 readings below f_1 and 5

readings above f_1 , at least 5 readings in the mid band, at least 5 readings below f_2 and 5 readings above f_2 .

11. Plot graphs of AV versus Frequency, f and /or M, dB versus Frequency, f on a semi log graph paper. From the graph determine: Mid –band - gain, Lower and Upper Cut-off frequencies and Band width. Compute the GBW product and verify with answer obtained earlier.

Observation: Use the tabular column separately for each circuit

V_{in} (P-P) = V

$AV = V_O$ (P-P)/ V_{in} (P-P)

$M = 20 \log (AV)$, dB

Frequency In Hz	100	200	300	350	400	500	600	700	800	1K
	2K	3K	5K	8K						

V_O (P-P) in

Volts

AV

M, dB, (AV in dB)

Frequency In Hz	10K	20K	30K	50K	100K	200K	300K	400K	500K	600K
	700K	800K	900K	1M						

V_O (P-P) in Volts

AV

M, dB, (AV in dB)

Expected graph

Result:

EXPERIMENT 4

CLASS B PUSH PULL AMPLIFIER

Aim: Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency.

Components and equipments required: Complementary symmetry transistors SL100 and SK100, Resistors – 47K Ω - 2nos, 4.7K Ω - 1no, 1K Ω - 2nos, 10K Ω pot - 1no, 0.01 μ F – 2 nos, Load box or DRB, Multimeter, Connecting wires and Bread board/Spring board with spring terminals

Theory: Complementary-Symmetry Class B Amplifier uses complementary or matching pairs of power transistors. The Class B amplifier circuit uses complimentary transistors for each half of the waveform. Main disadvantage of class B type push-pull amplifiers is that they suffer from an effect known commonly as Crossover Distortion.

Transistor takes approximately 0.7 volts (measured from base to emitter) to get a bipolar transistor to start conducting. In a pure class B amplifier, the output transistors are not "pre-biased" to an "ON" state of operation. Hence part of the output waveform which falls below this 0.7 volt window will not be reproduced accurately as the transition between the two transistors. The output transistors for each half of the waveform (positive and negative) will each have a 0.7 volt area in which they will not be conducting resulting in both transistors being "OFF" at the same time.

Illustrating Cross-over distortion

Circuit Diagram:

Procedure:

1. Wire the circuit as in circuit diagram
2. Give a sine wave input of frequency 1 KHz and amplitude 2 V p-p and observe the output.

3. Note down the peak to peak output voltage for each values of input voltage as indicated in the tabular column.
4. Note down the output voltage for every step of input voltage which is shown in the tabular column.
5. Calculate the efficiency using the formulae given in the table.

Let $R_L = 1K\Omega$, $V_{cc} = 10V$,

$$\frac{P_o}{P_i} \times 100 \%$$

Observation:

V_i (p-p) in Volts	V_o (P-P) in Volts	$V_M = V_o(P-P)/2$ in Volts	$\frac{P_o}{P_i} \times 100 \%$
2			
4			
6			
8			
10			
12			
14			
16			
18			
20			

Result:

EXPERIMENT 5

DARLINGTON EMMITTER FOLLOWER

Aim: Realize BJT Darlington Emitter follower with and without bootstrapping and determine the gain, input and output impedances.

Components and equipments required: Transistor (SL100), Resistor, DC regulated power supply, voltmeter, Ammeter, signal Generator, CRO and capacitors.

Theory: A very popular connection of two BJTs for operation as one super beta transistor is the Darlington connection. The main feature of Darlington connection is that the composite transistor acts, as a single unit with a current gain is equal to product of individual current gains. To make the two

transistors Darlington pair, the emitter terminal of the first transistor is connected to the base of the second transistor and the collector terminals of the two transistors are connected together. The result is that emitter current of the first transistor is the base current of the second transistor.

Design:

Let $V_{CC} = 12 \text{ V D.C.}$; $I_{C2} \approx I_{E2} = 6\text{mA}$, $h_{fe1} = 50$, $h_{fe2} = 100$;

Choose $V_{CE2} = V_{CC} / 2 = 12/2 = 6\text{V}$;

$I_{B2} = I_{C2}/h_{fe2} = 6000/100 = 60\mu\text{A} = I_{C1}$;

$I_{B1} = I_{C1}/h_{fe1} = 60/50 = 1.2\mu\text{A}$

$R_E = (V_{CC} - V_{CE2})/I_{E2} = 6\text{V} / 6\text{mA} = 1000 \Omega$

Assume $R_3 = 1\text{K}$, then $R_3 I_{B1} = 1.2 \text{ mV}$.

$V_{AG} = V_{AB1} + V_{BE1} + V_{BE2} + V_{E2}$

$= R_3 I_{B1} + V_{BE1} + V_{BE2} + V_{E2}$

$= 1.2 \text{ mV} + 0.7 \text{ V} + 0.7 \text{ V} + 6\text{V}$

$= 7.4012 \text{ V}$

With $R_2 = 1 \text{ K}$, $I_{R2} = V_{AG}/R_2 = 7.4012 \text{ mA} = 7401.2 \mu\text{A}$, let $R_2 = 1 \text{ K}$

There fore, $I_{R1} = I_{R2} + I_{B1} = 7401.2 + 1.2 = 7402.4 \mu\text{A}$

$R_1 = (V_{CC} - V_{AG})/I_{R1} = 12 - 7.4012 / 7402.4 \mu\text{A} = 621.258\Omega$; let $R_1 = 680 \Omega$ Choose $C_{C1} = C_{C2} = 0.47 \mu\text{F}$.

Circuit Diagram: Darlington Emitter follower with bootstrapping. (Remove CB for circuit without bootstrapping)

Procedure:

To measure Voltage Gain

1. Connect the circuit as shown in the figure
2. Switch on the power supply and set $V_{CC} = +12 \text{ V}$.
3. Measure the DC Voltages using CRO or Multimeter and record.

V_{CE1} V_{BE1} V_{CE2} V_{BE2} V_{E2}

Assumed 6V 0.7V 6V 0.7V 6V

Obtained

4. Apply a sine wave voltage from the Function Generator.
5. Observe the o/p V_o . Measure and record V_i and V_o . Compute and enter the voltage gain, $A_V = V_o/V_i$ in the table.

Voltage gain with bootstrap

V_i V_i, Max
 V_o
 A_V

Record V_i, Max , The maximum input you can apply for undistorted output as the “Maximum Signal handling capacity” of the Emitter follower.

6. Repeat the experiment after disconnecting the capacitor C_B in branch AB, i.e.; just remove the Bootstrapping capacitor, C_B . Now you have taken away the Bootstrapping.

Voltage gain without bootstrap

V_i V_i, Max
 V_o
 A_V

To measure Input Impedance Z_i :

1. Connect the circuit as shown below.
2. Set the DRB to minimum (0Ω). Apply a 10 KHz sine wave signal of amplitude 1V (p-p) or any suitable value to get an undistorted output.
3. Measure V_o (p-p). Let $V_o = V_a$ (say) with DRB value = 0
4. Increase DRB value in steps till $V_o = V_a/2$. The corresponding DRB value gives Z_i .
5. Repeat the experiment by disconnecting C_B , the bootstrapping capacitor.
6. Compare the two input impedance values you have measured.

To measure output impedance, Z_o :

1. Connect the circuit as shown in figure
2. Set the DRB to its maximum resistance value. Apply a 10 KHz sine wave of amplitude 1V (p-p) or any suitable value to get undistorted output
3. Measure V_o (p-p), $V_o = V_b$ without DRB connection or DRB value at Max.
4. Decrease DRB value in steps till $V_o = V_b/2$. The corresponding DRB value gives Z_o .
5. In this part of the experiment, it is likely that the o/p wave form may get distorted as the DRB value is decreased. Then, V_i has to be set to a lower value and the steps to be repeated. Note carefully that the answer will be wrong if you take readings with distorted output.
6. Repeat the experiment by disconnecting the Bootstrapping capacitor.

Result:

1. Voltage Gain with Boot Strap. :
2. Voltage Gain with Boot Strap. :
3. Input Impedance, Z_i , with Bootstrap. :
4. Input Impedance, Z_i , without Bootstrap. :
5. Output Impedance, Z_o , with Bootstrap. :
6. Output Impedance, Z_o , without Bootstrap. :
7. Current Gain, A_i , With Bootstrap. :
8. Current Gain, A_i , Without Bootstrap. :

$$V_i = Z_i \times I_i, V_o = Z_o \times I_o \quad \therefore A_i = (I_o/I_i) = AV \times (Z_i/Z_o)$$

EXPERIMENT 6

SERIES VOLTAGE REGULATOR

Aim: Conduct an experiment on Series Voltage Regulator using Zener diode and power transistor to determine line and load regulation characteristics.

Components and equipments required: SL100 transistors (2 Nos), Zener Diode IN4738A (8.2V) or IN4742A (12V), 0 – 30 V variable power supply, One Auto ranging

Theory: This circuit combines zener diode regulator and voltage follower. This combination will reduce the load effect and source effect to a great extent. The output voltage is $V_0 = V_Z - V_{BE}$. As input voltage changes, the zener voltage remains same hence the output voltage also remains same. If the output voltage increases, the decreased base-emitter voltage causes transistor to conduct less, thereby reducing the output voltage. Consequently, the output voltage is maintained at a constant level.

Design:

$$V_Z = 8.2 \text{ V};$$

$$I_{Z\min} = 1.0 \text{ mA};$$

$$\text{For 2N3055 (Silicon)} = 20 - 70,$$

$$I_{C\max} = 15\text{A},$$

$$P_{D\max} = 115\text{W}$$

$$V_{IN} = 15 \pm 3\text{V}$$

$$V_{OUT} = V_Z - V_{BE} = 8.2 - 0.7 = 7.5\text{V}$$

$$V_{CE\max} = 18 - 7.5 = 10.5\text{V},$$

$$I_{C\max} = 115/10.5 = 10.9\text{A}$$

Let the load current vary from 2.5mA to 250mA. ie. $I_{L\min} = 2.5 \text{ mA}$ and $I_{L\max} = 250\text{mA}$

For $I_{L\max} = 250\text{mA}$, with $h_{FE} = 20$, $I_B = 250/20 = 12.5\text{mA}$

$$R = (V_{INmin} - V_Z) / I_R,$$

$$I_R = I_{Bmax} + I_{Zmin} = 12.5 + 1 = 13.5 \text{ mA},$$

$$R = 3.8 / 13.5 = 281 \Omega \quad \text{let } R = 270 \Omega$$

Wattage of R:

$$P_R = (V_{R,max})^2 / R = 9.82^2 / 220 = 0.437 \text{ W}, \quad \frac{1}{2} \text{ W resistor is sufficient.}$$

Range of R_L :

$7.5 \text{ V} / 250 \text{ mA}$ to $7.5 \text{ V} / 2.5 \text{ mA} = 30 \Omega$ to $3 \text{ K}\Omega$ Vary R_L in the range 50Ω to $2.5 \text{ K}\Omega$ Wattage of load resistors: $50 \Omega - 1.125 \text{ W}$ – Use $50 \Omega - 1.5 \text{ W}$ all other resistors should have wattage appropriately ($7.52 / R_L$). Usage of DRB is suggested

Circuit Diagram:

Procedure:

1. Measure and record the values of V_0 and R_L keeping $V_{in} = 15 \text{ V}$

R_L $2.5 \text{ K}\Omega$ $2.0 \text{ K}\Omega$ $1.5 \text{ K}\Omega$ $1 \text{ K}\Omega$ 800Ω 500Ω 250Ω 100Ω 50Ω

V_0

$$I_0 = V_0 / R_L$$

2. Plot a graph of V_0 Vs I_0 .

Load regulation is calculated as below: $\text{Regulation} = (V_{NL} - V_{FL}) / V_{FL}$.

3. Adjusting R_L so as to maintain output current constant, Tabulate the following and find "Line regulation". (Here you will need an ammeter in series with R_L)

$$I_0 = \text{Constant (Say } 20 \text{ mA)}$$

V_{IN} 12 V 13 V 14 V 15 V 16 V 17 V 18 V

V_0

Percentage of line regulation =

Result: Line regulation =

Load regulation =

EXPERIMENT 7

HARTLEY AND COLPITTS OSCILLATOR

Aim: Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation.

(a) Hartley Oscillator (b) Colpitts Oscillator

LC oscillators are generally used as RF oscillators since they generally used to create high frequency oscillations. In Hartley and Colpitts oscillator an LC tank circuit is used for selection of frequency of oscillation. A voltage divider biased common emitter amplifier is used as amplifier. The amplifier and tank circuit together provides a phase shift of 360 degrees to satisfy Barkhausen criterion.

HARTLEY OSCILLATOR

Components and equipments required: Transistor SL 100, Resistors 470Ω, 1KΩ 10KΩ and 33 KΩ; Capacitors 0.1μf - 3nos, Discrete inductances 100 μH – 2 nos, Capacitor 470 pF – 2nos, Power supply, CRO, Connecting wires etc.

Design:

BJT- Amplifier design is same as given in Common Emitter Amplifier.

Tank Circuit Design: Oscillator Frequency $f = \frac{c}{\text{Leq.}} = \frac{1}{\sqrt{L1 + L2}}$

Assume $f = 500 \text{ KHz}$. With $L1 = L2 = 100\mu\text{H}$, we get $\text{Leq.} = L1 + L2 = 200\mu\text{H}$

$\text{Leq.} \cdot C = \frac{1}{(2\pi f)^2} = \frac{1}{(2\pi \times 500 \times 10^3)^2} = 10^{-12}$

This gives $C = \frac{1}{(\pi)^2 \times 200\mu\text{H}} \text{ pF} \approx 500\text{pF}$

Use $C = 470 \text{ pF}$

For this capacitance value $f = 518.6 \text{ KHz}$

Circuit Diagram:

Procedure:

1. Switch on the Power Supply and check the D.C conditions by removing the coupling capacitor CC1 or CC2.
2. Connect the coupling capacitors and obtain an output waveform on the CRO. If the o/p is distorted vary 1- KΩ Potentiometer (R3) to get perfect SINE wave.
3. Measure the period of oscillation and calculate the frequency of oscillation.
4. Compare the measured frequency with re-computed theoretical value for the component values connected. Observation:

Parameter	VRC	VCE	VE	ICQ = VRC / RC	VBE	VB
Assumed	4.8V	6 V	1.2V	4.5 mA	0.6 V	4.8V

Practical

Result: The frequency of oscillation is

COLPITTS OSCILLATOR

Components and equipments required: Transistor SL 100, Resistors 470Ω, 1KΩ 10KΩ and 33 KΩ; Capacitors 0.1μf - 3nos, Discrete inductances 100 μH – 2 nos, Capacitor 470 pF – 2nos, Power supply, CRO, Connecting wires etc.

Design:

BJT- Amplifier design is same as given in Common Emitter Amplifier.

1 C1C2

Tank Circuit Design: $f = \frac{1}{2\pi L C_{eq}}$ Where $C_{eq} = \frac{C1 C2}{C1 + C2}$

$$L = \frac{1}{4\pi^2 f^2 C_{eq}}$$

Given Oscillation frequency $f = 1 \text{ MHz}$

Assume $C1 = C2 = 470 \text{ pF}$ $C_{eq} = 235 \text{ pF} = 2.35 \times 10^{-10} \text{ F}$

1

Then, $L = \frac{1}{4\pi^2 (1 \times 10^6)^2 (2.35 \times 10^{-10})} = 119 \mu\text{H}$

?

Use $L = 100 \mu\text{H}$, For this value of L , $f = 1.04 \text{ MHz}$

Circuit Diagram:

Procedure:

1. Switch on the Power Supply and check the D.C conditions by removing the coupling capacitor CC1 or CC2.
2. Connect the coupling capacitors and obtain an output waveform on the CRO. If the o/p is distorted adjust 1- K Ω Potentiometer (R3) to get perfect SINE wave.
3. Measure the period of oscillation and calculate the frequency of oscillation.
4. Compare the measured frequency with re-computed theoretical value for the component values connected.

Observation:

Parameter	VRC	VCE	VE	ICQ = VRC / RC	VBE	VB
Assumed	4.8V	6 V	1.2V	4.5 mA	0.6 V	1.8 V

Practical

Result: The frequency of oscillation is

MENT 8

CRYSTAL OSCILLATOR

Aim: Design and set-up the crystal oscillator and determine the frequency of oscillation.

Components and equipments required: Transistor SL 100, Crystal – 2MHz, Resistors 470Ω, 1KΩ 10KΩ and 33 KΩ; Capacitors 0.1μf - 2nos, Power supply, CRO, Connecting wires etc.

Theory:

Crystal oscillators are used in order to get stable sinusoidal signals despite of variations in temperature, humidity, transistor and circuit parameters. A piezo electric crystal is used in this oscillator as resonant tank circuit. Crystal works under the principal of piezo-electric effect. i.e., when an AC signal applied across the crystal, it vibrates at the frequency of the applied voltage. Conversely if the crystal is forced to vibrate it will generate an AC signal. Commonly used crystals are Quartz, Rochelle salt etc.

Design:

Let $V_{CC} = 12V$;

$I_{CQ} = 4mA$;

$V_E = (1/10) V_{CC}$ to $(1/5) V_{CC}$;

$V_{CE} = 6V$; $h_{FE} = 100$.

To find R_E : Let us choose $V_E = 2V$

$R_E = V_E / I_{E} \approx V_E / I_C = 2V / 4mA = 500\Omega$; let

$V_{CC} = I_{CQ} R_C + V_{CEQ} + V_{EQ}$ $R_E = 470\Omega$

$R_C = (V_{CC} - V_{CEQ} - V_{EQ}) / I_{CQ} = 4.0V / 4mA = 1.0K\Omega$; $R_C = 1K\Omega$

Assume $R_2 = 10k\Omega$.

$V_B = V_E + V_{BE} = 2 + 0.6 = 2.6V$

$I_2 = \text{Current through } R_2 = V_B / R_2 = 0.26mA \text{ or } 260\mu A$

The base current $I_B = I_C / h_{FE} = 4mA / 100 = 0.04mA = 40\mu A$

($h_{FE} = \beta_{DC} = 100$, a working value; It varies from 50 to 280 for SL 100)

$I_1 = \text{Current through } R_1 = I_B + I_2 = 300\mu A$

$V_{R1} = V_{CC} - V_B = 12 - 2.6 = 9.4V$

$R_1 = V_{R1} / I_1 = 9.4V / 300\mu A = 9400 / 300 K\Omega = 31.33K\Omega$ $R_1 = 33K\Omega$

$C_E = C_C = 0.1\mu F$ (Arbitrary, any value which gives a reactance $< 10\Omega$ at Crystal frequency may be used. reactance of a Capacitor $X_C = (1/2\pi fC)$; For $C = 0.1\mu F$, $X_C = 0.8\Omega$ at 2 MHz) Circuit Diagram:

Procedure:

1. Switch on the Power Supply and before inserting the crystal check the D.C conditions by removing the coupling capacitor CC1 or CC2.
2. Insert the crystal and the coupling capacitors and obtain the output waveform on the CRO. If the o/p is distorted vary 1- K Ω Potentiometer (R3) to get perfect SINE wave.
3. Measure the period of oscillation and calculate the frequency of oscillation.
4. Compare with frequency marked on the crystal. Observation:

Parameter	VRC	VCE	VE	ICQ = VRC / RC	VBE	VB
Assumed	4.8V	6 V	1.2V	4.5 mA	0.6 V	1.8 V

Practical

Result:

MENT 9

JFET CHARACTERISTICS

Aim: Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.

Components and equipments required:

Supply 0 – 30V, 2 Numbers and Connecting wires and Bread board/Spring board with spring terminals.

Circuit setup diagram:

Procedure:

Set up the connections as indicated in the figure. V1 and V2 are Voltmeters (or multimeter) and A is ammeter (multimeter)

Follow the below procedure to obtain the drain characteristics:

1. Adjust the reading of V2 to
 - a. +0.5V by interchange the polarity VGG
 - b. 0V (Short the gate terminal to ground)
 - c. -1V, -2V and -3V.
2. For every constant VGG values (+0.5, 0, -1, -2, -3 etc) vary VDD voltage such that V1 is as indicated in the table below and record the corresponding readings of ID.

VGS = V2 = Constant (0.5V, 0V, -1V, -2V, -3V)

V1(VDS, V)	0.1	0.15	0.2	0.25	0.3	0.4	0.6	0.8	1.0	1.2	1.4
	1.6	1.8									

ID, mA

V1(VDS, V)	2	2.4	2.8	3.0	3.4	3.6	3.8	4.0	5.0	6	8
	10	12									

ID, mA

Follow the below mentioned procedure to obtain transfer characteristics:

1. Set VDS = 6V. This can be done by adjusting the reading of V1 to 6V.
2. Record the readings of ID for different values of V2 as indicated in the table. 3. Repeat step one and 2 for VDS = 9V and VDS = 12V

V2(VGS, V)	0	-0.2	-0.4	-0.6	-0.8	-1.0	-1.2	-1.4	-1.6	-1.8	-2.0
------------	---	------	------	------	------	------	------	------	------	------	------

ID, mA

V2(VGS, V)	-2.2	-2.4	-2.6	-2.8	-3.0	-3.2	-3.4	-3.6	-3.8	-4.0
------------	------	------	------	------	------	------	------	------	------	------

ID, mA

NOTE: For the drain characteristics, take at least 3 readings before and after the pinch-off starts (assumed pinch off voltage 4V) so that you will get a smooth graph. For the transfer characteristics, keep increasing |V2| till drain current becomes zero.

EXPECTED GRAPHS:

a) Drain Characteristics

b) Transfer Characteristics

From the graphs determine $g_m = (\partial I_D / \partial V_{GS}) | V_{DS} = \text{Constant}$

$r_d = (\partial I_D / \partial V_{DS}) | V_{GS} = \text{Constant}$

MENT 10

N-CHANNEL MOSFET CHARACTERISTICS

Aim: Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.

Components and equipments required: MOSFET IRF840, 100Ω Resistor, and 2 Numbers of DC Power Supply 0 – 30V, and Connecting wires and Bread board/Spring board with spring terminals.

Circuit setup diagram:

Procedure:

Follow the below mentioned steps to obtain the Drain Characteristics

1. Set up the connections as indicated in the figure.
2. Keep both VGG and VDD at zero position.
3. By varying VGG set VGS to some value (slightly greater than the Threshold voltage determined from the transfer characteristics) Say 3.0V
4. Increase VDS by varying VDD gradually and note down the corresponding meter readings as shown in the table.
5. Repeat the steps 3 and 4 for VGS=3.2V and VGS = 3.4V

6. Plot the graph of ID Vs VDS

.. TABLE – Drain Characteristics VGS = V2 = 3.0 (3.2V, 3.4V)

VDS =V1, V	0.2	0.4	0.6	0.8	1.0	1.5	2.0	3.0	5.0	10	12
	15	18	20								

ID , mA

Follow the below mentioned steps to obtain the Drain Characteristics

1. Set up the connections as indicated in the figure.
2. Keep both VGG and VDD at zero position.
3. Vary the VDD and set VDS = 5V.
4. Increase VGS by varying VGG gradually and note down the corresponding meter readings as shown in the table.
5. Note down the minimum value of VGS for which drain current starts flowing and record VTH =
6. Repeat for VDS = 10V and 15V.
7. Plot the graph of ID Vs VGS

. TABLE – Transfer Characteristics VDS = V1 = 5V (10V, 15V)

VGS =V2, V	1.0	2.0	2.8	2.9	3.0	3.1	3.2	3.3	3.4	3.5	3.8
	4.0	4.2	4.5								

ID, mA

Expected graphs:

Drain Characteristics

Transfer Characteristics

From the graphs determine $g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right) | V_{DS} = \text{Constant}$

$r_d = \left(\frac{\partial I_D}{\partial V_{DS}}\right) | V_{GS} = \text{Constant}$

MENT 11

JFET/MOSFET AMPLIFIER

Aim: Design, setup and plot the frequency response of Common Source JFET/MOSFET amplifier and obtain the bandwidth.

Components and equipments required: JFET – BFW10, Resistors - 180 Ω , 1K Ω , 10K Ω and 1M Ω , Capacitors 47 μ f, 0.1 μ f and 0.047 μ f, Power Supply, 10Hz – 3MHz Signal generator, CRO, Connecting wires and Bread board/Spring board with spring terminals.

Design:

For BFW10 Junction FET specifications are as below:

$V_{DS\ max} = 30\ V$, $V_{GS\ off} = -8\ V$, $I_{DSS\ min} = 8\ mA$, $I_{DSS\ max} = 20\ mA$

Choose $I_{DSS} = (Min + Max)/2 = (8 + 20)/2 = 14\ mA$,

$V_P = Max/2 = -4\ V$ and $g_m = 3.5\ to\ 6.5\ m\ mhos$

Quiescent-Conditions: $I_{DQ} = I_{DSS}/2 = 7\ mA$, Let $I_{DQ} = 5\ mA$. $V_{DD} = 12\ V$, $V_{DSQ} = V_{DD} / 2 = 6\ V$ Using these values, we get

$$V_p = I_{DQ} R_s$$

$R_s = I_{DQ} / I_{DSS} \times V_{DSQ} = 0.3219\ K\Omega$ let $R_s = 330\ \Omega$

With this choice of R_s , $V_S = R_s I_{DQ} = 1.65\ V$

$$R_D = (V_{DD} - V_{DSQ}) / I_{DQ} = 0.87\ K\Omega ; \quad \text{Let } R_D = 1.0\ K\Omega$$

R_G may be chosen arbitrarily but should be large enough such that overall input impedance is not affected much. Let $R_G = 1.0\ M\Omega$

$CC_1 = 1/2 \times f_1 R_i$ will be very small because of large R_i and chosen to be much larger so that it does not decide f_1 . Thus $CC_1 = 0.1\ \mu F$

Let $R_L = 10\ K\Omega$ and $f_1 = 300\ Hz$

Typical value of output admittance for BFW10, $g_d = 85\ \mu\ mhos$

That is, $r_d = 1/g_d = 12\ K\Omega$. Therefore $R_D || r_d \approx R_D = 1\ K\Omega$

Now, $CC_2 = 1/2 \times f_1 (R_D + R_L) = 0.0482\ \mu F$

Thus select $CC_2 = 0.047\ \mu F$

Choosing $X_C = R_S/10 = 18\Omega$ at $f_1/2 = 150\text{Hz}$, we get $C_S = 58.9\mu\text{F}$ let $C_S = 47\mu\text{F}$ or $C_S = 100\mu\text{F}$ Circuit Diagram:

Procedure:

1. Switch on the D.C. power supply and check the D.C. conditions without any input signal and record in table below:

Parameter	VDD	VRD	VDS	VS	IDQ	VGS
Assumed	12V	4.35V	6V	1.65V	5mA	-1.65V

Practical

2. Select sine wave input and set the input signal frequency $\geq 10f_1$ (Say = 10 KHz. This will be a convenient 'Mid – frequency').
3. Observe the input wave form and output wave form on a dual channel CRO.
4. Adjust the input amplitude such that the output waveform is just undistorted (or in the verge of becoming distorted). Measure the amplitude of the Input Signal now. This amplitude is the Maximum Signal Handling Capacity of your amplifier.
5. Decrease the input voltage to a convenient value such that the output is undistorted. Say 100mV. Measure the corresponding o/p voltage. Calculate midband gain, $AM = V_o (p-p) / V_{in} (p-p)$.
6. Keeping the input voltage constant, go on reducing the frequency until the output voltage reduces to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Lower Cut-off frequency (f_1).
7. Keeping the input voltage constant, go on increasing the frequency until the output voltage decreases to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Upper Cut-off frequency (f_2).
8. Thus you have pre-determined f_1 and f_2 . Find the amplifier band width, $BW = f_2 - f_1$
9. Determine Gain Bandwidth product (GBW product) which is a Figure of Merit of your amplifier as $GBW = AM \times BW$.
10. Now repeat the experiment by recording values of output voltage versus frequency keeping the input voltage at a constant value convenient to you. You should take at least five readings below f_1 and 5 readings above f_1 , at least 5 readings in the mid band, at least 5 readings below f_2 and 5 readings above f_2 .

11. Plot graphs of AV versus Frequency, f and /or M, dB versus Frequency, f on a semi-log graph paper. From the graph determine: Mid –band - gain, Lower and Upper Cut-off frequencies and Band width. Compute the GBW product and verify with answer obtained earlier.

Vin (P-P) =Volts (Constant)

Frequency

In Hz 100 200 300 350 400 450 500 600 800 1K

VO(P-P) in Volts

AV

M, dB

(AV in dB)

Frequency

In Hz 2K 3K 5K 8K 10K 20K 30K 50K 100K 200K

VO(P-P) in Volts

AV

M, dB

(AV in dB)

requeency

In Hz 300K 500K 800K 1M 1.5M 1.8M 2M 2.5M 2.8M 3M

VO(P-P) in Volts

AV

M, dB

(AV in dB)

$A_V = V_O (P-P) / V_{in} (P-P)$ (It is a ratio of two voltages. No units); $M = 20 \log (A_V)$, dB Expected Graphs:

Plot of Voltage Gain A_V versus frequency

EXPERIMENT 12

R C PHASE SHIFT OSCILLATOR USING FET

Aim: Design and set-up the RC-Phase shift Oscillator using FET, and calculate the frequency of output waveform.

Components and equipments required: Junction FET BF862, Resistors 27Ω , $1K\Omega$ and $56K\Omega$ - 3 nos. and a $10K$ pot; Capacitors $100\mu f$, 1000 pf - 3nos, Power supply, CRO, Connecting wires etc.

Design:

For RC Phase Shift Oscillator using FET, Barkhuasen Criterion gives:

1) $|A| \geq 29$

2) $f = 10$ Hz

To satisfy (1), we need $A = \geq 56$ with $f = 10$ Hz, where $f = 1 / (2\pi RC)$. Usually R_D will be small (1 K to 10K) and to achieve the desired gain, we need an FET that has a large g_m . BF862 satisfies this condition with minimum $g_m = 35$ mS. So BF862 is chosen.

$$\text{Let } V_{DD} = 12V, I_D = 1mA$$

I_{DSS} varies from sample to sample. A convenient value would be

$$(I_{DSSMin} + I_{DSSMax}) / 2 = (10 + 25) / 2 = 17.5 \text{ mA}$$

Thus choose $I_{DSS} = 18$ mA. Further, use $V_p = -0.8$ V

Compute R_S using

$$\text{Choose } R_S = 560\Omega$$

$$\text{Choose } V_{DSQ} = V_{DD} / 2 = 6V. \text{ Then } V_{RD} = V_{DD} - V_{DS} - V_S = 12 - 6 - 0.56 = 5.44 \text{ V}$$

$R_D = V_{RD}/I_D = 5.44 \text{ V} / 1 \text{ mA} = 5.44 \text{ K}\Omega$.
KHz

Choose $R_D = 5.6 \text{ K}\Omega$ Let β and Let $f = 1$

Then

Choose $C_S = 47 \mu\text{F}$

For the feedback network:

Let $R = 5.6 \text{ K}\Omega$. Then

Choose $C = 0.01 \mu\text{F}$

With this choice of components, the frequency of oscillation will be

Circuit Diagram:

Procedure:

1. Make the circuit connections for the base amplifier portion only and measure the Q – conditions and record.

	VDD	VDS	VS	VRD	ID=VRD/RD
Design Values	12V	6V	0.6V	5.6V	1mA

Measured Values

2. Wire the Feedback network.
3. Connect the 1K / 10K pot between A and D (or between B and G) and adjust to get a sine wave form on the CRO. (You can connect the pot in series with bypass capacitor, C_S , as shown in the diagram and try)
4. Measure the frequency of oscillation and compare with the theoretical value.
5. Measure the output amplitude. Does this vary if VDD is varied?

Result:

Viva Questions:

1. What is a rectifier?
2. Why do you need a rectifier?

3. What is the meaning of ripple?
4. What are the different filter configurations available to remove these ripples?
5. What is the value of ripple factor for a Full wave rectifier? Is this different for a Bridge rectifier?
6. What is the value of efficiency for a Full wave rectifier? Is this different for a Bridge rectifier?
7. Write the equation for the ripple factor of a full wave rectifier with C – filter.
8. Write the equation for V_{dc} of a full wave rectifier with C – filter.

Viva Questions:

1. Explain the concept of Zener breakdown?
2. How depletion region gets thin by increasing doping level in Zener diode?
3. State the reason why an ordinary diode suffers avalanche breakdown rather than Zener breakdown?
4. Give the reasons why Zener diode acts as a reference element in the voltage regulator circuits.
5. What type of biasing must be used when a Zener diode is used as a regulator?
6. What are the advantages of the Series feedback regulator?

Viva Questions:

1. Why do you need high input impedance?
2. What is the input impedance of an ordinary emitter follower?
3. Indicate the methods by which you can increase the input impedance of the emitter follower.
4. State Miller's theorem. How does this theorem help you in your circuit?
5. Draw the AC equivalent circuit of the Boot strapped emitter follower and show how the effect of the bias resistors is altered.

Viva Questions:

1. What is an amplifier?
2. What kind of bias should be applied for the transistor to act as an amplifier?
3. What are the bias conditions for transistor to be in (a) Saturation region? (b) Cut – off region? (c) Active region?
4. What is early effect? Is it an advantage or a disadvantage?

5. Mention different types of transistor biasing methods.
6. Which biasing method provides stabilization against variations in I_{CO} , β , V_{BE} ?
7. What are the different methods of coupling amplifier stages?
8. What is the advantage of RC Coupling?
9. Write an expression for the mid – band voltage gain for a single stage RC coupled amplifier.
10. Which are the components that affect the lower cut – off frequency?
11. Which are the components that affect the upper cut – off frequency?
12. Does the Emitter by – pass capacitor have any effect on the cut – off frequencies? Which cut – off frequency will it affect?
13. Write an expression for the voltage gain of the amplifier in the low frequency region in terms of mid-band gain and lower cut – off frequency
14. Write an expression for the voltage gain of the amplifier in the high frequency region in terms of mid-band gain and upper cut – off frequency.
15. What are the merits and de-merits of the R – C Coupled amplifier?
16. Write equations for the Gain, Input Impedance, Output Impedance, Upper Cut-off frequency and Lower Cut-off frequency of a feedback amplifier in terms of these quantities without feedback.
17. What makes the Input impedance with feedback to be different than the theoretical value?
18. What are the effects of ‘Negative feedback’? Just mention the effects by writing relevant equations.

Viva Questions:

1. What are the classifications of Field effect transistors?
2. Write the symbols for an N – Channel JFET and a P – Channel JFET.
3. What are the advantages of Field effect transistors?
4. What decides the maximum signal handling capacity of the FET RC coupled amplifier?
5. What are MOSFET’s?
6. What is the difference between MOSFET and BJT?
7. What are the types of MOSFET?
8. What is the difference between depletion mode and enhancement mode MOSFET’s?
9. How does n-drift region affect MOSFET?

10. How MOSFET's are suitable for low power high frequency applications?
11. What are the requirements of gate drive in MOSFET?
12. What is rise time and fall time?
13. What is pinch off voltage?
14. In which region the MOSFET is used as a switch?
15. Which parameter defines the transfer characteristics?
16. Why MOSFET's are mainly used for low power applications?
17. How MOSFET is turned off?
18. What are the advantages of vertical structure of MOSFET?
19. What are the merits of MOSFET?
20. What are demerits of MOSFET?
21. What are the applications of MOSFET?

Viva Questions:

1. What are power amplifiers?
2. How are power amplifiers different from conventional Voltage or Current amplifiers?
3. Define the efficiency of a power amplifier.
4. What are the efficiencies of R-C Coupled Class A, Single ended Class A and Class B power amplifiers?
5. What are the disadvantages of Class B power amplifiers with center tapped transformer?
6. What is cross-over distortion? What is the reason for this distortion?
7. How this distortion can be eliminated? Explain.
8. What are 'complimentary symmetry' transistors?
9. Write the applications of Power amplifiers.

Viva Questions:

1. What is an oscillator? What kind of feedback is used in oscillator circuits?
2. What are the conditions to be satisfied in order to produce oscillations? What are these conditions called?

3. Write other versions of Hartley oscillator circuits.
4. What are Relaxation Oscillators?
5. Why LC oscillators are not suitable for Audio frequencies?